An Alternative Approach to Bit Error Rate Testing (BERT)

Cost Effective Method Yields Better "Real World" Results

The traditional method of design margin testing in serial data communication systems is to employ a specially designed bit error rate (BER) tester. While BER testers have proven effective, they are typically expensive and they do not always exercise the system under test with the same level of noise or using the same data patterns that will be seen by the system in the field. This can leave some design flaws undetected. To ensure that all design flaws are found prior to product release, it is best to test the system while it is under a real world load—including eye-pattern variances and worst case data patterns.

This article discusses a test methodology that may be applied to a wide range of data communication systems and devices which transmit data over a serial bus. This test methodology may be part of the design verification process or it may be used to qualify substitute components after the product has been released to production. The example below describes how the methodology was used to debug a Fibre Channel switch. The test setup incorporates a Fibre Channel host bus adapter (HBA), a PC housing the HBA and running test software, and two signal generators. The test methodology was used to uncover a latent design flaw that had not been detected using a BER tester.

Figure 1 shows a typical serial interface of a data communications system.

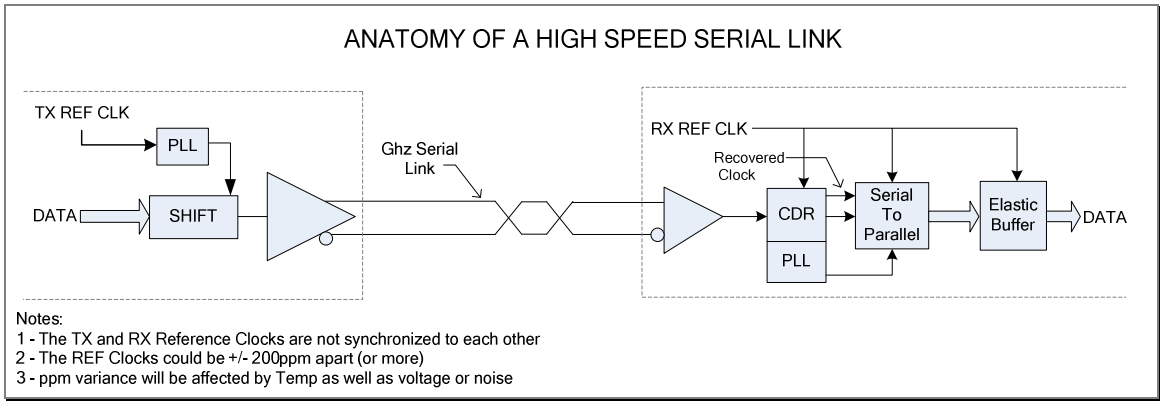

Figure 1. Anatomy of the serial interface of a data communications device.

Test Setup

A Fibre Channel switch was tested for data reliability as part of the design verification process. The test configuration is shown in the figure 2 .

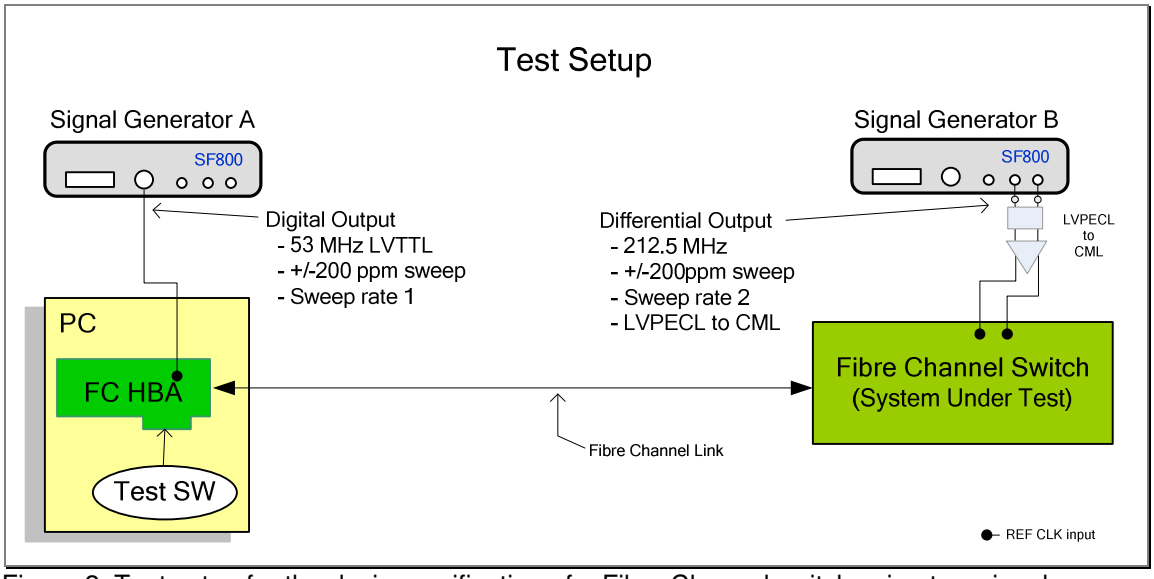

Figure 2. Test setup for the design verification of a Fibre Channel switch using two signal generators.

The test setup utilizes two signal generators with highly programmable sweep capabilities that are able to drive multiple clock types and input levels. Signal Forge signal generators were chosen because they provide a digital output with programmable voltage level, as needed to drive the Fibre Channel HBA, and they provide the differential output needed by the system under test (SUT), a Fiber Channel switch with a 2 Gbit/sec data rate.

The frequency of the HBA and the SUT were programmed into the respective signal generators and the frequency sweep range was set for the worst-case +/- ppm range for each device as specified by the Fibre Channel standard. The rate of change of the frequency was set to a unique value for each signal generator in order to prevent the HBA and SUT from switching in unison. The following equation was used to determine the deviation range:

$$\text{ppm} \times F(\text{in MHz}) = \text{deviation (in Hz)}$$

The HBA required a 53 MHz, 1.8V digital clock source while the switch required a 212.5 MHz differential clock source. The digital output of signal generator A was connected directly to the HBA using a short length of coax wire. Signal generator B was connected to the Fibre Channel switch through a voltage converter. The voltage converter is needed since switch requires a CML voltage level and the signal generator output is LVPECL. The conversion was accomplished by AC-coupling the SUT's input to the signal generator's differential output and adjusting the Vtt voltage level to achieve the proper voltage parameters. The voltage conversion circuit is depicted in Figure 3.

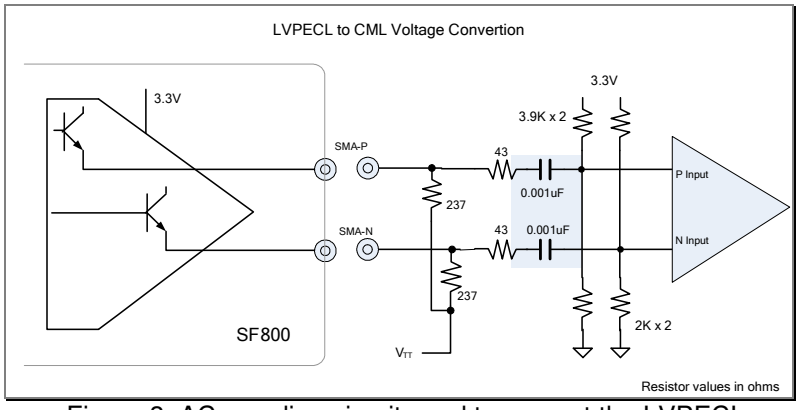

Figure 3. AC-coupling circuit used to convert the LVPECL differential output voltage to CML for input to the SUT.

Test Procedure

First, the integrity of each component of the system under test was verified individually. This was done by sweeping the clock of each component from min to max. After successfully completing the component test, a test of the interconnected system was conducted by sweeping the reference clock input of both the HBA and the SUT simultaneously.

It was important to keep the inputs to the SERDES PLL REFCLK of the HBA and the SUT from changing in unison because if the two clocks were allowed to change at the same rate, margin testing would not occur.

To keep the signal generators from changing in unison, the output of signal generator A and signal generator B were programmed for different deviation, step size and step rate. With the two clocks changing at different rates they are never in phase allowing all corner cases to be found. This setup allowed the interconnected system to be tested in a real world environment and verified that the entire system maintained the required setup and hold under all conditions.

Next, the signal generators were set to displace the center frequency by +/-200 ppm as specified by the Fibre Channel standard.

While the HBA and SUT clock inputs were being sweep, test software was reading and writing data through the interconnected system. The test software was written in Visual Basic using standard operating system handles for I/O operations. The software was programmed to send, retrieve and compare data of variable size files, in a worst case data pattern, from the PC, through the HBA, to the switch and back.

Results

After running the test for twelve hours, a data transmission error was detected indicating a data pattern sensitivity in the SUT—a bug not detected by the BER tester—which would require a silicon spin of the switch ASIC to correct. In order to reduce the impact to the product delivery schedule, it was critical that the time to reproduce the bug be reduced significantly. To do this, ten of the test beds described above were set up and run simultaneously. This enabled the design team to reproduce the error in a just a few minutes.

This methodology saved two months of development time and found a critical bug during the development cycle rather than after product release.

Notes

1. The signal generators provide a digital clock output that is programmable for amplitude (1.2V, 1.8V and 3.3V) as used by most systems.
2. The signal generators saves waveform configurations in non-volatile memory and reloads and starts one of the saved configuration automatically. This makes it easy to run the clock-margining test repeatedly without reprogramming.
3. The signal generators were allowed to power up and a TCXO soak of 1 hour was used in order to achieve maximum frequency stability.

About the Author

Steven Robalino is an electrical engineer with over twenty years experience designing circuit boards and chips in the storage and telecommunications industries. He is currently the chief technology office and co-founder of Signal Forge. Mr. Robalino was previously vice president of engineering for the QLogic Corporation, Management Products Group. Prior to that he was vice president of engineering and co-founder of Silicon Design Resources, a developer of semiconductors for the server and storage markets which was acquired by QLogic. Mr. Robalino also held engineering management positions, responsible for ASIC and circuit board development, at AMCC and Distributed Processing Technology (now Adaptec).

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About Signal Forge

Signal Forge was founded in 2004 with the goal to market high performance test equipment in small, affordable packages. The company takes an innovative approach to solving a problem that the founders faced at semiconductor and systems companies in the past—the need to accelerate product development schedules on a limited budget.

From experience, the founders determined that one of the most effective ways to reduce the development schedule is to reduce the test and debug cycle time. And the best way to accomplish that is to run multiple test beds simultaneously. The problem is that the high performance test equipment currently available is large and expensive, making it unaffordable for most labs to buy enough units to build multiple test environment setups.

Signal Forge uses an innovative 'design for cost and portability' approach to its product designs. It's first product, the Signal Forge 800 Signal Generator, achieves the company's goal of a high performance product in a small, affordable package.

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About the Signal Forge 800

The Signal Forge 800 Digitally Synthesized Signal Generator, is a high performance device with a 1 GHz range in a small, affordable package. It combines frequency generation, frequency sweep,

frequency modulation, amplitude modulation and arbitrary modulation into a single unit. Outputs include: AC coupled, differential and a digital output supporting 3.3V, 2.5V and 1.8V voltage levels.

Features include: - 1000 Hz to 800 MHz output, usable to 1GHz - Sine wave and square wave - FM, AM, FSK, OOK, ASK and arbitrary modulation modes - Fast, programmable linear sweep mode - External and internal control of Start, FSK, OOK and ASK - Synthesized signal and TCXO provide outstanding performance, precision and accuracy - Menu driven, embedded Wave Manager software – Small package (8.5in x 5.5in x 1.5in).

A wide, stable frequency range with multiple outputs in a small, easy to use package combine to make the Signal Forge 800 the ideal tool for RF and digital electronics test and development applications.