SIGNAL FORGE

Application Note

Converting Differential LVPECL to LVDS and CML

Applicable Products

SF1000
SF100E
SF800
SF800E

Description

The Signal Forge Digitally Synthesized Signal Generators provide a differential clock output that conforms to the LVPECL standard. While LVPEC is a widely used standard, there are other differential signaling standards in use today including LVDS and CML. This application note addresses how to convert the LVPECL differential output to LVDS and CML.

Interface

Two methods may be implemented:

- AC Coupled interface – requires the receiver to provide its own center bias (a resistor divider or a V_{TT} voltage source).
- DC Coupled interface – requires less components, but the designer must check and adjust for proper voltage swing

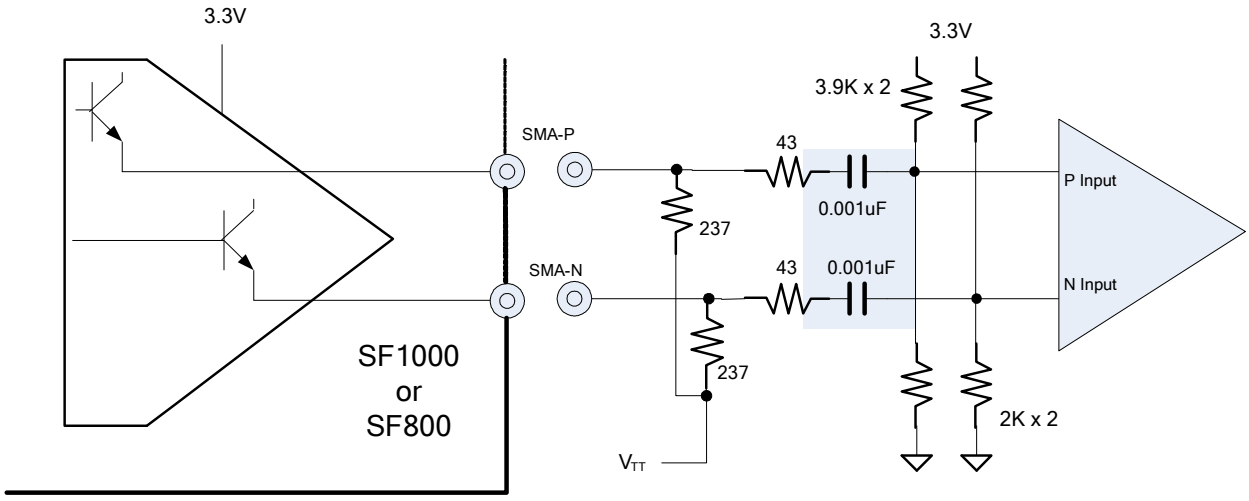
The AC coupled interface, described below, is ideal and simple to implement.

AC Coupled Interface

This interface is ideal for clock signals (or highly repetitive signals). The LVPECL driver requires a DC path to V_{TT}. The following items must be considered:

- The coupling capacitor must provide no AC resistance at the lowest frequency of operation
- The output voltage swing can be adjusted by varying the VTT voltage slightly
- The output voltage swing can be reduced by the use of series resistors.
- The DC voltage levels of the receiver should be within the voltage input high common mode range (VIHCMR).
- Proper layout design practices must be followed in order to minimize reflections and assure reliable operation.

The diagram below shows this method of interfacing in detail:



Resistor values in Ohms

LVPECL Interface Characteristics

Parameter	Value	Unit	Operational Voltage
V_{OH} – Max.	2.480	V	3.3V
V_{OH} - Typ.	2.355	V	
V_{OH} – Min.	2.230	V	
V_{OL} – Max.	1.680	V	
V_{OL} – Typ.	1.555	V	
V_{OL} – Min.	1.430	V	

LVPECL outputs measured with 50 Ohm termination and V_{TT} of 1.3V

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