



Application Note

Testing Digital Systems

Applicable Products

Models
SF1000
SF1000E
SF800
SF800E

Description

The Signal Forge Digitally Synthesized Signal Generators may be used to test the design margin of a digital system by varying the clock input to the system under test from min to max. This is an excellent test to verify that the system maintains the required setup and hold under all conditions.

Operation

The SF1000/800 provides a digital clock output that is programmable for amplitude (1.2V, 1.8V and 3.3V). Additionally, the SF1000/800 may be programmed to sweep the clock output from a minimum frequency to a maximum frequency using a predetermined rate of change. The frequency range can be set to be a +/- ppm range or some other worst-case range as defined by the system designer.

The SF1000/800 saves the last configuration in non-volatile memory and restarts using that saved configuration (optional feature). This makes it easy to setup this clock-margining test inside environmental chambers since a console setup is not needed every time the system is powered up.

Implementation Notes

The digital output of the SF1000/800 behaves just like any other digital clock driver or oscillator. A point-to-point connection to a single receiver is best in order to avoid reflections. The SF1000/800's output is configured as depicted below:

