SIGNAL FORGE

Application Note

Testing High Speed Serial Busses

Applicable Products

Models
SF1000
SF1000E
SF800
SF800E

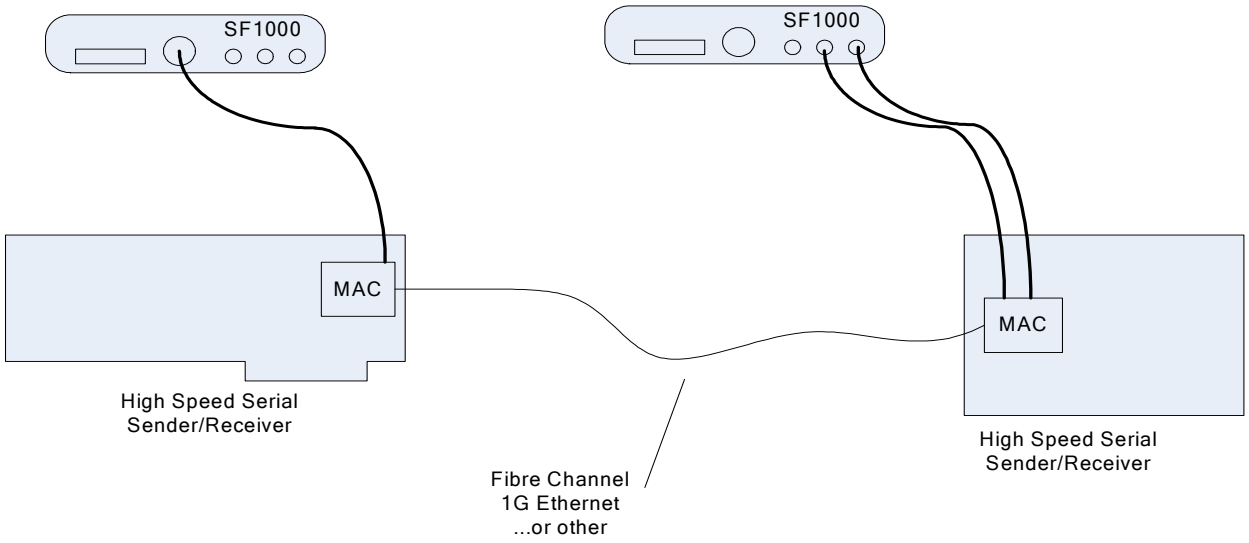
Description

When connecting devices or systems with high-speed serial busses, it is critical that data integrity between the connected devices be maintained. The difficulty is that while the devices are running at the same frequency, they are driven from different clock sources, are not the same phase and are not at the same ppm offset.

Since the designer of the serial bus devices must guarantee operation of the sender and receiver over these variations as well as over manufacturing variances, it is imperative to test many samples as possible, including 'batch' variances. This application note describes how the Signal Forge Digitally Synthesized Signal Generators may be used to verify your serial bus device's design and interoperability, while *minimizing the test time*.

Operation

This method of testing a serial bus system uses the SF1000/800 as a clock generator. The SF1000/800's low cost enables the designer to setup and operate several test beds, reducing test time and allowing many different clock margin tests to be performed in parallel. The SF1000/800 includes a clock output ppm test feature useful for testing clock margin in digital or analog systems at different and varying rates of change. The implementation is shown in the block diagram below:



Implementation Notes

The block diagram above shows two serial bus devices connected to each other. The clock source of each serial bus device is being driven by an SF1000/800. The SF1000/800 is programmed to:

- Drive the proper center frequency
- Increase/decrease the clock frequency by a preprogrammed range (or ppm value)
- Program the rate of change -individual SF1000/800 devices would be programmed to different rates of change in order to keep the serial bus devices from getting into a 'beat' where they all change in unison.

The high speed serial bus devices should be set to run data integrity test programs using worst-case patterns to test data integrity as well as bit error.

In the example above, one of the serial bus devices requires a digital output clock which is provided by the Digital Output of the SF1000/800. The other uses a differential clock input, which is provided by the Differential Outputs of the SF1000/800.